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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,268	06/23/2004	Masahiko Ando	92372	9828

7590 08/08/2006

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EXAMINER	
HITESHEW, FELISA CARLA	

ART UNIT	PAPER NUMBER
1722	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,268	ANDO ET AL.	
	Examiner	Art Unit	
	Felisa C. Hiteshew	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14,16 and 17* is/are allowed.

6)☒ Claim(s) *1-13,15,18 -20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *see attached paper*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The PTOL 1449 has been received, reviewed and considered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-5, 9-13,15 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over European 0 889 510 A1 (EP'510 A1) in view of Adachi, et al "Reduction in Grown-In Defects by High Temperature Annealing".

EP'510 A1 teaches an annealing method of silicon single crystal wafers capable of increasing the number of silicon single crystal wafers processed. Various studies were conducted for preventing dislocations and slips in high-temperature annealing environments. A large volume of wafers, e.g. 100, was placed into the same furnace at the same time. As results, a stack of up to 10 wafers can be treated as a unit or "group" horizontally or inclined (column 4, lines 48-58 and column 5, lines 1-5). During the ramping up process to a temperature in excess of 1,100*C when annealing is performed by maintaining a fixed temperature or a plurality of fixed temperatures can be provided, wherein the temperatures range form 500*C to 900*C. During the ramp down process, wherein temperature are in excess of 1100*C, the temperature can be dropped back to the 500*c to 900*C range (column 6 lines 1-27). Large numbers of wafers may be processed simultaneously, and that grown-in defects, which are the source of surface layer COP, as well as internal grown-in defects, can be reduced or eliminated in each wafer by heat treatment at over 1,250*C ranging from 1280*C to 1380*C (col. 6, lines 29-38). The DZ layers are to a depth of 30um from the wafer surface, but in regions deeper than that, oxygen precipitates are around 10^5 to 10^6 /cm^2.

The difference being that EP'510 A1 does not teach a method for eliminating defects from single crystal wafers wherein the initial oxygen concentration in the single crystal silicon is no more than 14 x 10^{17} (atoms/cc) along with the oxidation treatment in the course of raising the temperature to the level at which high temperature heat treatment is performed.

Adachi, et al teaches a method for the reduction of grown-in defects by high temperature annealing. The grown-in defects were formed owing to aggregation of excess vacancies during the CZ crystal growth method. The defects appeared at the wafer surface as pits called crystal originated particles (COPs) after mirror polishing and SCI cleaning. In order to decrease the density of grown-in defects and improve gate oxide integrity, slow cooling in the temperature range around 1000*C was performed. Hydrogen annealing at 1200*C was used to eliminate COPs. The silicon wafers were, 100. oriented 150mm in diameter, boron-doped CZ grown crystals with an oxygen concentration of 14.0×10^{17} atom/cm^3 (columns 1 and 2, page 350). The wafers were annealed at 1200, 1250 and 1300*c for two hours in argon or oxygen ambient. For wafers annealed at 1300*C in an argon ambient, the number of LPDs decreased remarkably and remained constant, independent of the depth. In addition, all observed LPDs were not pits, but particles. The grown-in defects with sizes of over 0.12 um in diameter were eliminated by 1300*C (column 2, page 351). It would have been obvious to one of ordinary skill in the art to modify and optimize the process and product parameter limitations, as taught by EP'510 A1 with the process and product parameter limitations, as taught by Adachi, et al. The motivation being that a variety of annealing could be applied to silicon single crystal wafers, making it possible to prevent dislocation and slips in order to provide effective uniformity to all wafers manufactured.

A reference is good not only for what it teaches by direct anticipation but also for what one of ordinary skill might reasonably infer from the teachings. In re Opprect 12 USPQ 2d 1235, 1236 (CAFC 1989); In re Bode 193 USPQ 12; In re Lamberti 192

USPQ 278; In re Bozek 163 USPQ 545, 549 (CCPA 1969); In re Van Mater 144 USPQ 421; In re Jacoby 135 USPQ 317; In re LeGrice 133 USPQ 365; In re Preda 159 USPQ 342 (CCPA 1968).

Allowable Subject Matter

5. Claim14,16 and 17 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: The most relevant prior art references were those that were submitted by the applicants. However, they do not teach nor fairly suggest singularly or in any combination thereof a method for eliminating defects from single crystal silicon, in which single crystal silicon that has been manufactured by the CZ method and that has not undergone an oxidation treatment is subjected to an ultra high temperature heat treatment by being heated to an ultra high temperature in an oxygen gas atmosphere or an atmosphere containing oxygen gas, and then cooled, thereby eliminating any void defects present in the single crystal silicon, wherein void defects present in the single crystal silicon are eliminated by adjusting parameters comprising the initial oxygen concentration in the single crystal silicon, the oxygen partial pressure of the atmosphere during heating up to the ultra high temperature, the oxygen partial pressure of the atmosphere during the ultra high temperature heat treatment, and the temperature at which the ultra high temperature heat treatment is performed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Felisa Hiteshew whose telephone number is (571) 272-1463. The examiner can normally be reached on Mondays through

Thursday from 5:30 AM to 4:00 PM with Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta, can be reached on (571) 272-1316. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-1463.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system. see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866- 217-9197 (toll-free).

FELISA HITESHEW
PRIMARY EXAMINER
AU1738